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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/657,797	09/08/2003	William C. Moyer	SC13071TH	1577

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EXAMINER	
PAN, DANIEL H	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 02/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/657,797	MOYER ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10,12,13,15-22,25,27,28 and 30-43* is/are rejected.

7)☒ Claim(s) *8,9,11,14,23,24,26 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 06/14/05, 3/24/05, 01/16/04, 09/08/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-43 are presented for examination,

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claim 1 provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/657,331 Although the conflicting claims are not identical, they are not patentably distinct from each other because although the copending claim 1 does not recite the fires offset and second offset as claimed in the current claim 1, it would have been obvious to one of ordinary skill in the art to use the first offset and second offset as claimed because the copending claim also taught a specifier for specifying the number of data elements to be transferred between the memory and the two registers (see

copending claim1, lines 9-16), which would have been recognizable by one of skill in the art that the number of data elements had to be determined based on two pointers for referencing the two registers , and these two could have been two starting location values, such as offsets , or the like .

3. Claim 1 provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/657,510 Although the conflicting claims are not identical, they are not patentably distinct from each other because although the copending claim 1 did not recite the first offset and second offsets as claimed, it would have been obvious to one of ordinary skill in the art to use the first offset and second offsets because the copending claim 1 also taught the determination of the data element size in memory separate and independent from the size of data element in the register (see copending claim1), which would have been recognizable by one of ordinary in the art that independent and separate size in the memory from the register could have used a starting location value separate from the starting location of the register ,, which would have been a second offset.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2,6,7,10,12,16,17, 19,20,21,25,27 are rejected under 35 U.S.C. 102(b) as being anticipated by Inagami et al. (4,760,545).

5. As to claim 1, 16, Inagami taught at least :

a) a memory for storing operands (see the main storage for storing the vector data elements and transferring the data into the vector registers in col.1, lines 51-58, col.3, lines 29-32),

b) at least one general purpose register (see the vector registers VR) , and

c) processor circuitry for executing one or more instructions (see load/store instruction format in fig.4b), at least one of the one or more instructions for transferring data elements between the memory (main memory) and the at least one general purpose register (VR) wherein one of the one or more instructions specifies: (a) a first offset [VIR] between data elements within a first portion of successive data elements in the memory; (b) a first number of data elements [L] to be transferred between the memory and the at least one GPR; and (c) a second offset [D1] between the first portion (the portion of element s being transferred started at D1) and a second portion [VAR] of data elements (see the top address VAR) in the memory.

6. As to claim 2, Inagami VIR (the distance or length) also specify the size of a data element (see VIR value when the L=1).

7. As to claim 6, Inagami also included total number of data elements to be transferred (se L in fig.4, see col.4, lines 54-56).

8. AS to claim 7,17, Inagami 's one of one or more instructions also transferred between the memory and both registers (see the transfer between the memory and plurality of registers in col.3, lines 28-33).

9. As to claim 10, 19,20,21,25, Inagami also specified number of data elements to be transferred between memory and each register (see L in col.4, lines 53-58, see fig.4b [L]).

10. As to claims 12,27, Inagami also used the offset (see D1) once while transferring the first number o f data elements (see D1 with corresponding L in col.4, lines 45-65).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 3-5 , 18, 34,37, 40,43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inagami (4,760,545) in view of Omoda et al. (4,825,361) .

AS to claims 3-5 , 18, 34,37, 40,43, Inagami did not specifically tech the specified size of data element separate and independent from the specifying size of data in memory as claimed . However, Omoda disclosed that the size of the vector elopement specified in the memory was independent from the size in the register (see col.). It would have been obvious tom one of ordinary skill in the art to use Omoda in Inagami for specifying the intendment and separate size in memory form the size specified in the register as claimed because the use of Omoda could provide the control ability of Inagami to adapt to different vector data element size based on the system requirements, such as the specific data width of the system bus, and therefore it would allow Inagami the flexibility to rearrange the vector data element based on the bus width, and because Inagami also taught

12. Claims 13, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inagami (4,760,545) in view of Betker et al. (6,052,766).

13. As to claims 13,28, limitations of parent claims already discussed above not be repeated herein. Inagami did not specifically show the circular buffer as claimed . However, Betker taght a vector system including a circular buffer (see col.15, lines 1-18). It would have been obvious to one of ordinary skill in the art to use Betker in Inagami for including the circular buffer as clamed because the use of Betker could provide Inagami the ability to reuse the data elements in a repeated cycle, therefore, increasing the data storage access in a predefined sequence, and it could be done by predefining the port width of circular buffer of Betker into the configuration file of

Inagame so that the particular R/W port of Betker circular buffer could be recognized by Inagami, and because Inagami's teaching of the vector iteration (see the iterated do loop of vector operation in fig.1) was a suggestion of the need for providing a buffer in a predetermined loop sequence , or the like, for sorting vector data elements for respective values of the loop control variable accessed directly for the do loop vector operation, thereby minimized the overall latency due to the circuit overheads, and for doing so, provided a motivation.

14. Claim 15, 30, 31, 32 ,33,35,36,38,39,41,42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inagami (4,760,545) in view of Blomgren et al. (6,898,691)

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15. As to claims 15, 30, 31,32,33, 35, 38, 41, limitation of parent 16 have been discussed above. Inagami taught at least :

a) a memory for storing operands (see the main storage for storing the vector data elements and transferring the data into the vector registers in col.1, lines 51-58, col.3, lines 29-32),

b) at least one general purpose register (see the vector registers VR) , and

c) processor circuitry for executing one or more instructions (see load/store instruction format in fig.4b), at least one of the one or more instructions for transferring data elements between the memory (main memory) and the at least one general purpose register (VR) wherein one of the one or more instructions specifies: (a) a first offset

[VIR] between data elements within a first portion of successive data elements in the memory; (b) a first number of data elements [L] to be transferred between the memory and the at least one GPR; and (c) a second offset [D1] between the first portion (the portion of element s being transferred started at D1) and a second portion [VAR] of data elements (see the top address VAR) in the memory.

16. Inagami did not specifically show his instruction specified a radix specifier for implementing the data element transfer in bit reverse order (claim 16, 30, 31, reverse order for claims 32, 35 , 41) as claimed. However, Blomgren taught a vector system including instruction for specifying a radix and transferring data element in reverse order (see the radix reversal order col.9, lines 27-59, col.11, lines 34-42, see also col.6, ,lines 6-18 for transfer between memory and vector registers). It would have been obvious to one of ordinary skill in the art to use Blomgren in Inagami for including the radix for implementing the reversed bit transfer as clamed because the use of Blomgren could provide Inagami the capability to accept data in a predefined set of order , therefore, increasing the ability of Inagami for processing the vector operation with higher degree of complexity, and because one of ordinary skill in the art should be able to recognize the use of Blomgren into Inagami as Inagami sought the possibility to avoid reading and writing from a main memory (known to be slow) and effected the processing that the of the vector data referenced only once (see col.15, lines 35-52) , and Blomgren was looking for the solution for reducing the number of independent memory transfer (i.e. read/write) and improve the performance (col.2, lines 6-15),

therefore, both Inagami and Blomgren were directed to the same problem, and in doing so, provided motivation.

17. As to claims 36,39, 42 Inagami also included total number of data elements to be transferred (see L in fig.4, see col.4, lines 54-56).

The following are in effect only on the pending condition of the PDP set forth in this action.

18. Claims 8,9 ,23 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of specifying a total number of data elements to be transferred between the memory and both the first and second registers.

19. Claims 11 ,24 , 26 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of filing at least a portion of any remaining bit

locations either predetermined value if the total number of data elements transferred does not completely fill the second register.

20. Claims 14 , 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of the specifier the second offset used mo0re than once if the first number of data elements to be transferred is larger that twice the first portion of the dale elements to be transferred.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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